CLAIMS

What is claimed is:

1. A semiconductor structure comprising:

a substrate having a major surface;

at least one trench formed in said substrate extending from said major surface, said trench includes inner surfaces filled with conductive material which is electrically separated from said substrate by insulating material;

a first insulating layer disposed on said major surface above said trench, said first insulating layer having a first contact opening;

a first conductive layer disposed above said first insulating layer and in contact with said conductive material in said trench through said first contact opening;

a second insulating layer disposed above said first conductive layer, said second insulating layer having a second contact opening; and

a second conductive layer disposed above said second insulating layer and in contact with said substrate through said second contact opening.

2. The semiconductor structure as set forth in claim 1 further including a source layer disposed in said substrate extending from said major surface.

3. The semiconductor structure as set forth in claim 2 wherein said structure is a MOSFET structure having a source, a drain and a gate, said source includes said source

layer, said drain includes said substrate, and said gate includes said trench.

4. The semiconductor structure as set forth in claim 1 wherein said second conductive layer comprises a substantially rectangular shape disposed on said major surface of said substrate, wherein said rectangular shape of said second conductive layer having no elongated voids extended therein.

5. The semiconductor structure as set forth in claim 1 wherein said first insulating layer comprises silicon dioxide and said second insulating layer comprises borophosphorous silicon glass.

6. The semiconductor structure as set forth in claim 1 wherein said first and second insulating layers are made of material selected from a group consisting of silicon dioxide, borophosphorous silicon glass, and phosphorous silicon glass.

7. The semiconductor structure as set forth in claim 1 wherein said conductive material inside said trench comprises polycrystalline silicon.

8. The semiconductor structure as set forth in claim 1 wherein said first and second conductive layers comprise metal.

9. The semiconductor structure as set forth in claim 8 wherein said metal comprises aluminum.

10. The semiconductor structure as set forth in claim 1 wherein said first and second conductive layers are made of material selected from a group consisting of copper, aluminum, aluminum silicide, and alloy of aluminum, silicon and copper.

11. The semiconductor structure as set forth in claim 1 wherein said second conductive layer is plated with a metal layer.

12. The semiconductor structure as set forth in claim 11 wherein said metal layer comprises copper.

13. The semiconductor structure as set forth in claim 1 wherein said trench is a low-resistance trench, said semiconductor structure includes a plurality of said low-resistance trenches, said semiconductor structure further comprising a plurality of low-capacitance trenches disposed in said substrate, each of said low-capacitance trenches being disposed without said first conductive layer disposed thereabove and having a trench width substantially narrower than the corresponding trench width of said low-resistance trench, said low-resistance trenches and said low-capacitance trenches being disposed interleaving with each other in said substrate.

14. The semiconductor structure as set forth in claim 1 wherein said trench is elongated in shape.

15. A semiconductor structure comprising:
a substrate having a major surface;

a plurality of trenches formed in said substrate extending from said major surface, some of said trenches being orientated in a first direction and others of said trenches being orientated in a second direction, each of said trenches being filled with conductive material which is electrically separated from said substrate by insulating material;

an insulating layer disposed on said major surface above said trenches, said insulating layer having a plurality of contact openings positioned above said trenches along said first and second directions; and

a conductive layer disposed above said insulating layer and in contact with said conductive material in said trenches through said contact openings.

16. The semiconductor structure as set forth in claim 15 wherein said conductive layer includes criss-crossing segments disposed above said major surface of said substrate, some of said segments being orientated in said first direction and others of said segments being orientated in said second direction, each of said segments being disposed in substantial alignment with one of said trenches.

17. The semiconductor structure as set forth in claim 16 further including a source layer disposed in said substrate extending from said major surface.

18. The semiconductor structure as set forth in claim 17 wherein said structure is a MOSFET structure having a source, drain and a gate, said source includes said source layer, said drain includes said substrate, and said gate

includes said trenches.

19. The semiconductor structure as set forth in claim 15 wherein said conductive material inside said trench comprises polycrystalline silicon.

20. The semiconductor structure as set forth in claim 15 wherein said trenches are low-resistance trenches, said semiconductor structure further comprising a plurality of low-capacitance trenches disposed in said substrate, each of said low-capacitance trenches being disposed without said conductive layer disposed thereabove and having a trench width substantially narrower than the corresponding trench width of each of said low-resistance trenches, said low-resistance trenches and said low-capacitance trenches being disposed interleaving with each other in said substrate.

21. The semiconductor structure as set forth in claim 15 wherein said insulating layer is a first insulating layer, said contact openings are first contact openings and said conductive layer is a first conductive layer, said structure further comprising:

a second insulating layer disposed above said first conductive layer, said second insulating layer having a plurality of second contact openings; and

a second conductive layer disposed above said second insulating layer and in contact with said substrate through said second contact openings.

22. The semiconductor structure as set forth in claim 21 wherein said second conductive layer is plated with a

metal layer.

23. The semiconductor structure as set forth in claim 22 wherein said metal layer comprises copper.

24. The semiconductor structure as set forth in claim 21 wherein said second conductive layer being substantially rectangular in shape disposed on said major surface of said substrate, wherein said rectangular shape of said second conductive layer having no elongated voids extended therein.

25. The semiconductor structure as set forth in claim 24 wherein said first and second insulating layers are made of material selected from a group consisting of silicon dioxide, borophosphorous silicon glass, and phosphorous silicon glass.

26. The semiconductor structure as set forth in claim 21 wherein said first and second conductive layers are made of material selected from a group consisting of copper, aluminum, aluminum silicide, and alloy of aluminum, silicon and copper.

27. A semiconductor structure comprising:

a substrate having a major surface;

a plurality of trenches formed in said substrate extending from said major surface, some of said trenches being orientated in a first direction and others of said trenches being orientated in a second direction, each of said trenches being filled with conductive material which is electrically separated from said substrate by insulating

material;

a first insulating layer disposed on said major surface above said trenches, said first insulating layer having a plurality of first contact openings above said trenches along said first and second directions;

a first conductive layer having criss-crossing segments disposed above said major surface of said substrate, some of said segments being orientated in said first direction and others of said segments being orientated in said second direction, each of said segments being disposed in substantial alignment and in contact with one of said trenches through one of said first openings;

a second insulating layer disposed above said first conductive layer, said second insulating layer having a plurality of second contact openings; and

a second conductive layer disposed above said second insulating layer and in contact with said substrate through said second contact openings.

28. The semiconductor structure as set forth in claim 27 further including a source layer disposed in said substrate extending from said major surface, wherein said structure is a MOSFET structure having a source, a drain and a gate, said source includes said source layer, said drain includes said substrate, and said gate includes said trenches.

29. The semiconductor structure as set forth in claim 28 wherein said first insulating layer comprises silicon dioxide, said second insulating layer comprises borophosphorous silicon glass, said conductive material

inside said trench comprises polycrystalline silicon, and said first and second conductive layers comprise metal.

30. The semiconductor structure as set forth in claim 29 wherein said second conductive layer being substantially rectangular in shape disposed on said major surface of said substrate, wherein said rectangular shape of said second conductive layer having no elongated voids extended therein, thereby allowing bonding wires to be substantially unrestrictively attached onto said second conductive layer.

31. The semiconductor structure as set forth in claim 30 wherein said second conductive layer is plated with copper.

32. The semiconductor structure as set forth in claim 31 wherein said trenches are low-resistance trenches, said semiconductor structure further comprising a plurality of low-capacitance trenches disposed in said substrate, each of said low-capacitance trenches being disposed without said first conductive layer disposed thereabove and having a trench width substantially narrower than the corresponding trench width of each of said low-resistance trenches, said low-resistance trenches and said low-capacitance trenches being disposed interposing with each other in said substrate.